IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
SHERMAN DIVISION

STMICROELECTRONICS, INC., Plaintiff, v. SANDISK CORP., Defendant, Counterclaim Plaintiff, v. STMICROELECTRONICS, N.V., and STMICROELECTRONICS, INC. Counterclaim Defendants.	C.A. NO. 4:05CV45 Judge Michael H. Schneider Magistrate Judge Donald D. Bush Jury Trial Demanded

SANDISK CORPORATION'S REPLY CLAIM CONSTRUCTION BRIEF
FOR THE SANDISK PATENTS

I. THE '812 PATENT

A. AGREED TERMS

In addition to the agreed-to terms identified in ST's Response, the parties now agree on constructions for the following claim terms.

1. "effective threshold voltage level"/"effective threshold voltage level of the addressed cell"

The parties agree that these claim terms refer to the "minimum amount of voltage that must be applied to the control gate before the transistor is turned 'on' to permit conduction between its source and drain region."

2. "electrically interrogating the addressed cell"

The parties agree that this claim term refers to the "applying the appropriate voltages to the addressed cell to induce an electrical parameter."

B. SANDISK'S PROPOSED CLAIM CONSTRUCTION OF DISPUTED CLAIM TERM

1. "simultaneously comparing a resulting level of an electrical parameter of the addressed cell with a number of reference levels of two or more" (claim 15)

ST originally proposed, and SanDisk agreed, that this claim term means "comparing a particular electrical response of an addressed cell with multiple distinct reference levels at the same time." In its Responsive Brief, ST proposed a different construction, one that unnecessarily departs from the claim language. As a result, the parties now advance the following positions on this claim term:

SanDisk's Proposal	ST's Proposal
comparing a resulting level of an electrical parameter of an addressed cell with multiple distinct reference levels at the same time	comparing a resulting electrical parameter of an addressed cell with multiple distinct reference levels of that parameter at the same time

The claim term explicitly requires "comparing a resulting ***level*** of an electrical parameter ...," as reflected in SanDisk's proposed construction. ST's proposed construction, on the other hand, improperly removes the word "level." ST also attempts to rewrite the claim to add a requirement that the comparison be made with "reference levels of that [electrical] parameter." The claim requires that the comparison be made with "reference levels," but does not require that the reference levels be "of that parameter." ST

offers no reason to depart from the claim language. The claim language is clear and should control.

C. '812 PATENT CLAIM TERMS GOVERNED BY 35 U.S.C. § 112, ¶ 6

The parties agree that claim 22 of the '812 patent contains five means-plus-function limitations governed by 35 U.S.C. § 112, ¶ 6. Means-plus-function limitations are construed in two steps. First, the Court must identify and construe the function of the claim element.[1] Second, the Court must identify structure in the patent that corresponds to the claimed function.[2]

1. "means operably connected to said array for addressing a selected one or group of the plurality of memory cells" (claim 22)

The parties agree on the function of this limitation: "addressing one or more memory cells." The parties disagree, however, about what structure is disclosed in the '812 patent as corresponding to the recited function. The parties advance the following positions:

SanDisk's Proposal	ST's Proposal
Corresponding Structure: word line decode circuitry, bit line decode circuitry	*Corresponding Structure:* word line decode transistor, bit line decode transistor

Both parties agree that the '812 patent discloses addressing means that include circuitry for decoding the word line of the addressed cell and circuitry for decoding the bit line of the addressed cell. The parties disagree about what constitutes the decoding circuitry.

A preferred embodiment of the '812 patent is depicted in Figure 2e, which includes "Word Line Decode" and "Bit Line Decode" circuits. Referring to Figure 2e, the specification states, "In this circuit an array of memory cells has decoded word lines and decoded bit lines connected to the control gates and drains respectively of rows and columns of cells."[3] It further explains that the word line decoder and bit line decoder perform the function of addressing specific cells in the array to be programmed or read.[4]

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[1] *See Med. Instrumentation and Diagnostic Corp. v. Elekta AB*, 344 F.3d 1205, 1210 (Fed. Cir. 2003).

[2] *See id.* at 1211-12.

[3] '812 patent, col. 6, ll. 10-12.

[4] *Id.* at col. 1, ll. 44-49 ("A specific, single cell in a two-dimensional array of EPROM cells is ***addressed*** for reading by application of a source-drain voltage to source and drain lines in a column containing the cell being addressed, and application of a control gate voltage to the control gates in a row containing the cell being addressed."). *See also id.* at col. 6, ll. 28-43 ("A single short programming pulse is applied to both the selected word line and the selected bit line.").

ST argues that, because Fig. 2e depicts a single transistor symbol near the disclosed "Word Line Decode" and "Bit Line Decode," those circuits are limited to a single transistor each. ST misstates the disclosures and teachings of the '812 patent. The '812 patent plainly indicates that Figure 2e depicts the circuitry for the preferred embodiment as used in one of the many Flash EEPROM cells that make up a memory cell array. Figure 2e shows an ***example*** of a segment of a circuit "to implement the multistate storage concept ***in conjunction*** with an array of Flash EEPROM transistors."[5] For ease of understanding, Figure 2e illustrates operation of one cell (out of many) of the array, as shown by the singular figure labeled "FLASH EEPROM CELL." Figure 2e shows the "Word Line Decode" and "Bit Line Decode" signals and the respective transistors to which the signals are sent for addressing the memory cell (these are the single transistors to which ST would limit the decoder structure). Each cell of the array has its own set of these components, which are part of the structure for "addressing one or more memory cells."

No further disclosure of decoder circuitry was necessary. A person of ordinary skill in the art would understand that the reference to "Word Line Decode" and "Bit Line Decode"—in the context of addressing multitudes of rows (word lines) or columns (bit lines) of the entire array—is a reference to the signals coming from a word line decoder and a bit line decoder used to coordinate the overall addressing process.[6] As the Federal Circuit has explained, fuller disclosure of the decoder circuitry is unnecessary because decoder circuits were well known to those of ordinary skill in the field of the '812 patent.[7] Accordingly, the proper construction of this claim term refers to "word line decode ***circuitry***" and "bit line decode ***circuitry***," not to specific transistors that form only a portion of the decoder structure.

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[5] *Id.* at col. 6, ll. 7-9.

[6] Figure 2e is simply a high level illustration of the array and does not illustrate, as is typical in the art, all of the logic associated with decoding. Indeed, as the prior art cited during prosecution of the '812 patent evidences, decoder structures feeding into Figure 2e were well known to those skilled in the art and were often shown using high-level depictions. For instance, U.S. Patent No. 4,051,354, which was cited during the prosecution of the '812 patent and is therefore considered intrinsic evidence, discusses decoder circuitry used to address memory cells. '354 patent, col. 6, ll. 3-25; Figs. 1 and 2, attached as Exhibit 9. Other patents cited patents similarly discuss decoding circuitry and, in fact, refer to it as "ordinary." *See, e.g.,* U.S. Patent No. 5,386,388, col. 6, ll. 38-41 ("Through ordinary decoding, a row decoder selects a word line in the array. Likewise, a column in the array is selected using a column decoder."), attached as Exhibit 10; U.S. Patent No. 4,527,251, col. 6, ll. 45-47 ("The address section 207 includes circuits which decode, generate and distribute address signals required for initialization and read/write memory selection."), attached as Exhibit 11; U.S. Patent No. 4,281,398, col. 3, ll. 47-58, attached as Exhibit 12.

[7] *See S3 Incorporated v. nVIDIA Corp.*, 259 F.3d 1364, 1370-71 (Fed. Cir. 2001).

Furthermore, ST's proposed recitation of a single transistor to perform each of the word line decode and bit line decode functions ignores the claim limitation's express requirement that the addressing means be capable of addressing "a selected one ***or group of*** the plurality of memory cells." By themselves, as taught in the '812 patent, the two transistors shown in Figure 2e are not used to select a group of the plurality of memory cells—they select a single cell.[8] SanDisk's proposed structure, however, is consistent with the '812 patent specification because it enables selection of a group of cells.

2. "programming means operably connected to said array for altering the charge on the floating gate of an addressed cell until its said effective threshold voltage is substantially equal to one of a plurality of effective threshold voltage levels in excess of two corresponding to a plurality of individual detectable states in excess of two" (claim 22)

The parties agree on the function of this limitation: "altering the charge on the floating gate of an addressed cell until its said effective threshold voltage is substantially equal to one of a plurality of effective threshold voltage levels in excess of two corresponding to a plurality of individual detectable states in excess of two." The parties disagree, however, about what structure is disclosed in the '812 patent as corresponding to the recited function. The parties advance the following positions:

SanDisk's Proposal	ST's Proposal
Corresponding Structure: programming control circuit, word line program/read pulse generator, bit line program pulse generator	*Corresponding Structure:* word line decode transistor, word line, word line program/read pulsing circuitry, bit line, bit line decode transistor, bit line program pulsing circuitry, and programming control circuitry, plurality of sense amplifiers, plurality of reference current sources, comparator, split channel cell

The '812 patent specification provides a concise description at column 6, lines 28-43 of how a four-state memory cell can be programmed. In that passage, and referring to Fig. 2e, the structures directly corresponding to the function of programming the cell are the programming control circuit (activated when programming is required), word line program/read pulse generator, and bit line program pulse generator (both controlled by the programming control circuit).

[8] *See Asyst Techs., Inc. v. Empack, Inc.*, 268 F.3d 1364, 1370-71 (Fed. Cir. 2001); *Micro Chemical v. Great Plains Chemical*, 194 F.3d 1250, 1258-59 (Fed. Cir. 1999).

ST's proposal includes the three structures identified above but also identifies additional components that are ***not*** directly responsible for "programming" the addressed cell, namely the word line decode transistor and bit line decode transistor shown in Fig. 2e.[9] Neither the world line decode transistor nor the bit line decode transistor perform the function of "altering the charge." Instead, the two transistors are parts of circuits used to address or access a memory cell. The fact that a memory cell is addressed during a program operation does not convert an addressing circuit into a programming circuit. ST's position is wrong as a matter of law, because it is improper under § 112, ¶ 6 to incorporate structures into a means-plus-function element, where the structures do not perform the recited function.[10]

ST argues that the phrase "until its said effective threshold voltage is substantially equal to one of a plurality of effective threshold voltage levels in excess of two corresponding to a plurality of individual detectable states in excess of two" requires inclusion of a plurality of sense amplifiers, plurality of reference current sources and a comparator. ST misreads the claim limitation. The limitation at hand claims a means to program the cell. But, ST converts this limitation into a means for "determining" when programming is needed—not the actual programming means itself. Indeed, the portion of the specification relied upon by ST for inclusion of the sense amplifiers, current sources and comparator, *i.e.*, '812 patent, col. 6, lines 28-43, explains that these structures are used to determine if the cell is in the correct state and "programming is required." The specification, however, goes on to explain that if programming is required the programming is done by the programming control circuit, word line program/read pulse generator, and bit line program pulse generator. ST's construction is wrong because the limitation simply does not call for structure to ***determine when*** to program; rather, the limitation requires structure that programs. The "means for determining" limitation urged by ST is not found in claim 22 and is not part of a proper construction.

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[9] As discussed in Section I(C)(1), above, SanDisk disagrees with ST's characterization of the word line decode circuitry and bit line decode circuitry as each being limited to a single transistor.

[10] *See Asyst Techs.*, 268 F.3d at 1370-71; *Micro Chemical*, 194 F.3d at 1258-59.

The final point of contention is whether the corresponding structure includes a split channel cell. Requiring a split channel cell is inconsistent with the claim because the memory cell is what is programmed, so the cell itself is not a part of the structure used to program. Furthermore, the cell is part of the array, not "operably connected to said array," and thus cannot be part of the structure. Moreover, nothing in the description of Fig. 2e references a split channel cell. Indeed, Fig. 2e generically refers to a "flash EEPROM cell." Finally, the preamble to claim 22 provides specific requirements concerning the structure of the memory cells found in the claimed system. To narrow the memory cell structure beyond what is recited in the preamble would improperly read in a limitation from the preferred embodiment.

3. "means operably connected to said array for determining the amount of current that flows through an addressed cell" (claim 22)

Although the parties agree that the recited function of this claim limitation is correctly stated as "determining the amount of current that flows through an addressed cell," the parties have a fundamental disagreement about the interpretation of that language. As a result, the parties disagree about what constitutes the corresponding structure. The parties' proposed constructions are as follows:

SanDisk's Proposal	ST's Proposal
Corresponding Structure: sense amplifiers	*Corresponding Structure:* word line, word line decode transistor, word line program/read pulsing circuits, bit line, bit line decode transistor, split channel cell

Central to the parties' dispute is whether the word "determining," as used in this claim limitation, refers to both ***inducing*** current to flow through the addressed cell and ***detecting*** the amount of current that flows through the addressed cell, or just ***detecting*** the amount of current flow. ST argues for the former; SanDisk advocates the latter. The claim language itself resolves the dispute: The claim limitation requires "determining," *i.e.,* detecting or measuring the amount of current through an addressed memory cell using means "connected to the array." It says nothing about inducing a current that can be determined, and ST's attempt to read in "inducement" or "application" of current is wrong. Because the claim requires only determination, *i.e.,* detection, of the amount of current, the structures that

perform that function are limited to the sense amplifiers which receive the output current, IDS, from the memory cell. Figure 2e depicts this arrangement.[11]

ST again seeks to include structures that go beyond what is necessary to perform the recited function. ST improperly attempts to limit the invention to a "split channel cell." First, the cell itself is part of the array, not "operably connected to said array" and thus cannot be a part of the structure. Claim 22's preamble[12] expressly describes the structure of cells required in the claimed system. The preamble does not recite a split channel cell. It merely states EEPROM cell. Further, the cell itself is not a structure for detecting current that flows "through an addressed cell." Therefore, it cannot be a "corresponding" structure under 35 U.S.C. § 112, ¶ 6.

ST also identifies the word line decode transistor and bit line decode transistor, but those structures are the part of the means that address a memory cell and do not determine the amount of current that flows through an addressed cell.[13] The word line and bit line simply carry signals; they do not perform the function of determining the amount of any such signal. As a result, it is improper to include them as corresponding structures under 35 U.S.C. § 112, ¶ 6.

4. "means including a number of sense amplifiers of two or more for simultaneously comparing the amount of current flowing in an addressed cell with said number of reference current levels, whereby the state of an addressed cell is rapidly read" (claim 22)

The parties agree the function recited in this means-plus-function limitation is "simultaneously comparing the amount of current flowing in an addressed cell with said number of reference current levels." The parties generally agree on the corresponding structures. The point of contention is that ST modifies the agreed upon structure (*i.e.*, reference current sources) with the functional language "producing different reference levels." The parties' respective proposed constructions are as follows:

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[11] *See also* Ashok K. Sharma, SEMICONDUCTOR MEMORIES: TECHNOLOGY, TESTING, AND RELIABILITY, 124 (IEEE Press 1997) (drain-to-source (I_{DS}) current from a memory cell is "***detected by the sense amplifier***" (emphasis added)), attached to SanDisk's Opening Brief as Exhibit 3.

[12] '812 patent, col. 12, l. 57 – col. 13, l. 3.

[13] *See* Section I(C)(1), above, (disagreeing with ST's use of "transistor").

SanDisk's Proposal	ST's Proposal
Corresponding Structure: plurality of sense amplifiers, plurality of reference current sources	*Corresponding Structure:* plurality of sense amplifiers, plurality of reference current sources producing different reference levels

ST commits legal error in its proposed construction. The function, which has been agreed to by the parties, requires simultaneous comparison between cell current and a number of reference levels. Any structure under 35 U.S.C. § 112, ¶ 6 must perform this recited function. The structure should not—and, indeed, cannot—change the function recited in the claim. ST's additional functional language "producing different reference levels" is not found in the claim and should be rejected. Further, it would be legal error to so limit the invention because nothing in the text or figures of the '812 patent limits the invention to a particular type of reference current source. SanDisk's proposed construction is not skewed by the unsupported functional language proposed by ST, and should therefore be adopted.

II. THE '808 PATENT

A. AGREED TERM

1. "subjecting the EEPROM cells . . . in parallel to erase voltages"

The parties agree that this term, found in claim 1, means "providing voltages suitable to erase the cells in the selected sectors simultaneously."

B. SANDISK'S PROPOSED CLAIM CONSTRUCTION OF DISPUTED CLAIM TERMS

1. "erase together all the enabled sectors" (claims 5 and 11)

The parties dispute the meaning of this claim term and advance the following positions:

SanDisk's Proposal	ST's Proposal
erase all of the selected sectors as a group in response to a single erase initiation command from the controller	erase all of the selected sectors as a group

The '808 patent highlights the importance of multi-sector erasure, whereby multiple selected sectors are erased "together." ST's proposed construction is incomplete because it fails to explain or describe what "together" means in the context of erasing multiple sectors. That meaning is clear from reading the '808 patent, though. The '808 patent specification explains that the invention is an

improvement over prior art systems, such as the Seeq model 48512,[14] that were able to erase only one sector at a time.[15] These systems could erase multiple sectors only by sequentially issuing multiple erase commands to the memory chips—one erase command for each sector.[16] ST's proposed construction seeks to encompass such prior art systems by rendering meaningless the word "together." Its ambiguous construction would arguably encompass prior art systems that issued multiple erase commands (one command per sector) erased sectors as a "group" and thus "together." Yet, as ST knows, it is improper to construe claims in a manner that covers prior art references distinguished in the specification.[17]

As indicated in SanDisk's Opening Brief, the erasure of enabled sectors can be simultaneous or sequential.[18] But in every case, what defines a group of sectors being "erased together" is the activity of the controller, which issues a single global erase command per group of sectors.[19] The additional language in SanDisk's proposed construction does not read in a limitation from the specification. Instead, it gives meaning to the word "together" and provides a bright line for distinguishing a group of sectors erased together in accordance to the specification and claims of the '808 patent from a "group" of sectors individually erased in a prior art system.

2. "register associated with individual ones of the sectors to tag its respective sector as enabled for erasure" (claim 6)

The parties dispute the meaning of this claim term and advance the following positions:

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[14] *Id.* at col. 4, ll. 43-50.

[15] '808 patent, col. 4, ll. 43-50.

[16] *Id.*

[17] *See, e.g., SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys.*, Inc., 242 F.3d 1337, 1343-44 (Fed. Cir. 2001); *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1159, (Fed.Cir.1998) (specification distinguished prior art as inferior and touted advantages of a conical shaped cup for use in an artificial hip device; "[s]uch statements make clear that the '589 patent discloses only conical shaped cups and nothing further").

[18] *See generally* SanDisk's Technology Tutorial for the SanDisk Patents (filed February 21, 2006) (depicting sequential erasure of selected sectors).

[19] *See* '808 patent, col. 5, ll. 43-51; *id.* at Fig. 4.

SanDisk's Proposal	ST's Proposal
an information storage circuit containing information denoting whether an associated sector is (or associated sectors are) selected for erasure	register in one-to-one correspondence with an individual sector in memory to uniquely identify its associated sector as enabled for erasure

ST improperly seeks to limit each register to a fixed one-to-one correspondence with a single sector in the array. No such requirement exists in the '808 patent specification or claims. Indeed, as expressly stated in the '808 patent prosecution history, the '808 patent allows for a single tag bit to correspond to more than one sector.[20]

ST knows its proposed construction is incorrect. In prior litigation in the International Trade Commission involving the '752 patent, which is the parent application to, and shares the same specification with, the '808 patent, the presiding administrative law judge rejected the argument that one-to-one correspondence is required when construing the claim language "individual register associated with each sector for holding a status to indicate whether the sector is selected or not." The ALJ found: "[T]here is no indication in the claim language or specification that the claimed invention is restricted to the preferred method of constructing registers and arranging them in an exclusive, one-to-one correspondence with the sectors."[21]

Without providing any documentary citations, ST argues that "[i]ndividual *bits* cannot physically be associated with multiple sectors."[22] Even assuming ST were correct, this argument is irrelevant to a proper construction because it encompasses only those situations that ST contends never occur.

3. "plurality of registers that individually contain a tag indicating whether an associated sector is enabled for erasure or not" (claim 12)

The parties dispute the meaning of this claim term and advance the following positions:

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[20] *See* Prosecution History for U.S. Patent App. Serial No. 08/407,916 ('808 patent); Request for Continuance of Prosecution, Attachment (Initial Determination) at 44-46 (Apr. 23, 1997), attached to SanDisk's Opening Brief as Exhibit 8.

[21] *Id.*

[22] ST's Responsive Claim Construction Brief at 22.

SanDisk's Proposal	ST's Proposal
information storage circuits each containing information denoting whether an associated sector is (or associated sectors are) selected for erasure	plurality of registers in one-to-one correspondence with individual sectors in memory to uniquely identify their associated sectors as enabled for erasure

This claim term differs from the preceding claim term only by reciting a plurality of registers, where the preceding claim term recites "register" in the singular. Accordingly, the arguments made in the preceding section apply to this term as well.

4. "setting a tag bit" (claims 18 and 19)

The parties dispute the meaning of this claim term and advance the following positions:

SanDisk's Proposal	ST's Proposal
setting a bit to indicate that the sector associated with the bit is (or sectors associated with the bit are) selected for erasure	setting a bit to indicate that the sector associated with the bit is selected for erasure

The sole remaining difference between the parties' proposed constructions for this claim term is whether a tag bit is limited to being in one-to-one correspondence with a single sector, as indicated by SanDisk's inclusion of the phrase "or sectors associated with the bit" where ST recites only "sector" in singular form. Tag bits are the digital information stored by the system to track whether sectors are enabled for erasure, such as, for example, in the registers recited in the preceding two claim terms. *See* Sections II(B)(2) and (3), above. Accordingly, resolution of the "one-to-one correspondence" issue affecting the preceding two claim terms will also resolve the parties' dispute concerning this claim term.

5. "clearing the tags"/"clearing tags"/"clearing the tag bits" (claims 1, 7, 13, 19)

The parties dispute the meaning of these related claim terms and advance the following positions:

SanDisk's Proposal	ST's Proposal
resetting the bits so that the bits no longer indicate that the respective sector(s) associated with each bit is (are) selected for erasure	resetting the bits so that the bits no longer indicate that the respective sector associated with each bit is selected for erasure

The parties disagree about whether an individual tag bit can correspond to more than one sector. The Court's resolution of this issue for the preceding disputed claim terms (*see* Sections II(B)(2), (3) and (4), above) will also resolve the parties dispute regarding these claim terms.

6. "a logic circuit configured to address and enable for erasure, in response to signals from the controller, any combination of a plurality of but less than all of said multiple sectors" (claim 5)

The parties dispute the meaning of this claim term and advance the following positions:

SanDisk's Proposal	ST's Proposal
a logic circuit on a memory chip that is responsive to signals from a controller and can enable for erasure any combination of sectors from the set of permissible sector-erase combinations; each combination must consist of at least two but less than all sectors	a logic circuit configured to select and enable for erasure, in response to signals from the controller, any combination of at least two but less than all sectors; each combination must consist of at least two but less than all sectors

The parties disagree about two issues concerning the claim term: (i) whether the logic circuit is located on the memory chip, and (ii) what is meant by "any combination of a plurality of but less than all of said multiple sectors." SanDisk's proposed construction provides guidance to the jury by expressly addressing both issues, while ST's proposed construction is silent.

Claim 5 requires that the controller and logic circuit be separate and distinct components in the system of the '808 patent, reciting the two structures as separate limitations. This claim language is consistent with the specification of the '808 patent, which consistently teaches that the inventions of the patent improve system performance through on-chip logic that frees the controller to do other tasks after the issuance of the global erase command.[23] Specifically, Figure 2 illustrates a Flash EEPROM system with multiple sectors selected for erase. A controller 31 is in communication with each of the Flash EEPROM memory chips through line 209. Figure 3A shows the on-chip logic (circuit 220) of each memory chip in Figure 2 that is configured to enable erasure of a combination of multiple sectors. As described at column 5, lines 43-48, after all the sectors have been selected for erase, "the controller then issues to the circuit 220 … a global erase command." After the command is issued, the memory "device will erase all the sectors that have been selected (*i.e.*, the sectors 211 and 213)" for erase.[24]

[23] '808 patent, col. 7, ll. 8-13.

[24] *Id.* at col. 5, ll. 43-48.

By having the on-chip logic take over once the controller issues the erase command, the flash memory of the '808 patent improves system performance by freeing up the controller to perform other tasks. For example, after issuing the global erase command but prior to completion of erasure, the controller can send new addresses to the chip for the next command following the multisector erase.[25]

The above performance enhancing feature is a key feature of the '808 patent. The prior art Seeq approach discussed and distinguished in the '808 patent at column 4, lines 43-50, does not possess this feature. The Seeq memory chip required the "time consuming sequential approach" that required a memory controller to go through an erase sequence over and over again for each sector until all desired sectors have been erased. The logic circuit of the '808 patent frees the controller by having the memory chip take over in response to a global erase command. The logic enables the erasure of a combination of selected sectors. Then, in response to the global erase command, the logic circuit, in conjunction with the erase circuit, erases the selected sectors.

SanDisk's proposed construction also recognizes that the combination of sectors selected for erasure must come from those sectors capable of being erased. Indeed, the patent identifies a significant advantage in being able to skip sectors, such as defective or unused sectors,[26] and to flexibly configure erasure in a manner that limits power consumption.[27] Accordingly, SanDisk's proposed construction refers to the "set of permissible sector-erase combinations." Such language does not improperly read in limitations from the specification but, instead, reflects the reality of how the system disclosed and claimed by the '808 patent operates.

7. "a logic circuit configured to enable erasure of any one of multiple different combinations of a plurality of but less than all of said multiple sectors" (claim 11)

The parties dispute the meaning of this claim term and advance the following positions:

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[25] *Id.* at col. 7, ll. 11-13.

[26] *Id.* at col. 6, ll. 43-55 ("Additional advantage is that if a sector is ***bad*** or is ***not used*** for some reason, that sector can be skipped over with now erase occurring within that sector.") (Emphasis added).

[27] *See id.* at col. 6, ll. 56-65 ("The flexibility in erase configuration of the present invention enables the adaptation of the erase needs to the power capability of the system.").

SanDisk's Proposal	ST's Proposal
a logic circuit on a memory chip that is responsive to signals from a controller and can enable for erasure at least two different combinations of sectors; each combination must consist of at least two but less than all sectors	a logic circuit that can enable for erasure at least two different combinations of sectors; each combination must consist of at least two but less than all sectors

Federal Circuit case law requires that a claim term appearing in multiple claims should be construed in a consistent manner absent a clear indication that the term is intended to have different meanings in the different claims.[28] Claims 5 and 11 recite a "logic circuit" that enables erasure of any one of multiple different combinations of a plurality but less than all of said multiple sectors. There is nothing in those claims to indicate that the term "logic circuit" should have a different meaning.

Although ST is correct that, unlike the "logic circuit" claim term found in claim 5, the instant claim term does not expressly state that the logic circuit operates "in response to signals from the controller," ST fails to identify any language in claim 11 that indicates that the logic circuit in that claim is not responsive to signals from a controller. One of the central ideas of the '808 patent is a system that allows the controller to issue a global erase command to the logic circuit and thereby pass on to the logic circuit responsibility for managing the erasure of the selected sectors so that the controller may turn to other activities.[29] Claim 11, read in light of the specification, indicates that the "logic circuit" of that claim has the same meaning as the logic circuit of claim 5. There is no intrinsic evidence to the contrary.

8. "designating a combinations" / "another combinations" (claims 16, 23)

The parties dispute the meaning of this claim term and advance the following positions:

SanDisk's Proposal	ST's Proposal
In claims 16 and 23, subpart (a), "designating a combinations" means "designating a combination." In claim 16, subpart (c), "another combinations" means "another combination."	more than one combination

[28] *See CVI/Beta Ventures, Inc. v. Tura L.P.*, 112 F.3d 1146, 1159 (Fed. Cir. 1997).

[29] *See* '808 patent, col. 7, ll. 7-13.

ST commits legal error by arguing that "designating ***a*** combinations" refers to designating more than one combination. Claims are interpreted as a whole, even if they may appear difficult to understand.[30] The language of claims 16 and 23 clearly indicate that the inventors only required a combination of designated sectors. In both claims, the element immediately following the language "designating ***a*** combinations" shows that the claim requires only one combination. Claims 16 and 23 recited "designating ***a*** combination" as the antecedent basis part (a) for subparts (b) and (c), which recite "*the* combination of sectors" (singular). Similarly, in subpart (d) of claim 16, the form of the word "combination" that follows the word "another" should be treated as singular because it refers to repeating singular steps (b) and (c).

Although the language of the claims sufficiently reveal their proper construction, the Court may wish to refer to the specification, which provides additional support for SanDisk's position.[31] Passages in the specification explain how a combination of sectors is enabled for erasure and then erased.[32] Figure 4 also reveals how a combination of sectors can be selected for erasure and then erased.

ST's alternative proposal of changing every instance of "combination" to "combinations" results in a tortured construction of those claims. The Court need not waste its time entertaining ST's hypothetical scenarios.

III. CONCLUSION

Based on the foregoing, SanDisk respectfully requests that the Court adopt SanDisk's proposed constructions.

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[30] *S3*, 259 F.3d at 1364.

[31] *See Interactive Gift Express Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("If [] the claim language is not clear on its face, then our consideration of the rest of the intrinsic evidence is directed to resolving, if possible, the lack of clarity.")

[32] *See* '808 patent, col. 6 ll. 20-28 ("[A]fter all sectors intended for erase have been tagged, the controller initiates an erase cycle to erase the group of tagged sectors."); *see also id.* at col. 5, ll. 43-51.

Dated: March 15, 2006

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies the foregoing document was filed electronically on March 15, 2006, pursuant to Local Rule CV-5(a) and has been served on all counsel who have consented to electronic service and on all other counsel by regular mail.

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